Electronic Version
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[CHIP PACKAGE AND SUBSTRATE]

Abstract

A chip package comprising a substrate, a lead frame, a chip, a set of bonded wires, a heat sink and a packaging material is provided. The substrate has a first metallic layer, a second metallic layer and a conductor. The first metallic layer is formed on a first surface of the substrate and the second metallic layer is formed on a second surface of the substrate. The conductor is formed on a lateral surface of the substrate. The first metallic layer is electrically connected to the second metallic layer through the conductor. The lead frame is attached on the first surface of the substrate and is electrically connected to the first metallic layer. The chip has a back surface attached to the lead frame or the first surface of the substrate. The chip is connected with the lead frame through the bonding wires. The heat sink is attached on the second surface of the substrate and electrically connected with the second metallic layer. The packaging material encapsulates the chip, the bonded wires and the lead frame.